REMARKS

Examiner K. Chen is thanked for the thorough examination and search of the subject Patent Application. Claims 1, 15, and 24 have been amended.

All Claims are believed to be in condition for Allowance, and that is so requested.

Reconsideration of the rejection of Claims 1-23 under 35 U.S.C. 112 is requested in view of Amended Claim 1 and in accordance with the following remarks.

Claim 1 has been amended to claim that all portions of the dielectric layer have a dielectric constant less than 2.5. It is believed that this amendment overcomes the new matter rejection. The Examiner says that "no etch stop layer is used with said dielectric layer" in Claim 15 is new matter. The Examiner is directed to the bottom of page 10 where, in the summary of the invention, it is stated that an "ultra low-k insulating material is used without an etch stop layer." It is believed that this statement provides the basis for the negative limitation in the claims.

Reconsideration of the rejection of Claims 1-23 under 35 U.S.C. 112 is requested in view of Amended Claim 1 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 102 or 35 U.S.C. 103 of Claims 1, 2, and 10-14 as being anticipated by or unpatentable over Hung et al is requested in view of Amended Claim 1 and in accordance with the following remarks.

A key feature of Applicants' invention is that it is very important not to use etch stop layers within low dielectric constant layers (see top of page 2 of the Specification). It is important that the dielectric constant of the dielectric layer through which the damascene opening is etched be less than 2.5. If an etch stop is used within the dielectric layer, the effective

dielectric layer will increase above 2.5. In Hung et al, a nitride etch stop layer 16 is used within the dielectric layer 14/16/20 (see col. 9, lines 7-10 and Figs. 5-10). While it is agreed that Hung et al teach the use of Black Diamond which has a dielectric constant less than 2.5, the silicon nitride etch stop layer will increase the effective dielectric constant to more than 2.5 (see the discussion on page 2). It is important that all of the dielectric layer have a dielectric constant less than 2.5, as now claimed in Claim 1. This is not true for Hung's dielectric layer 14/16/20 where the portion 16 has a dielectric constant greater than 2.5. The Examiner notes that Applicants' liner layer 18 is the same composition as Hung's etch stop layer. Applicants' liner layer is analogous to Hung's lower stop layer 12. It is the dielectric layer overlying this lower stop layer that is the object of this invention. The dielectric layer 22 in Applicants' invention and 14/16/20 in Hung et al is the layer through which the damascene opening is etched. In a later step (the second etching in Applicants' claims), the lower stop layer 12 or liner layer 18 is removed.

Reconsideration of the rejection under 35 U.S.C. 102 or 35 U.S.C. 103 of Claims 1, 2, and 10-14 as being anticipated by or unpatentable over Hung et al is requested in view of Amended Claim 1 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 3, 5, 7, 8, 15-18, and 21-23 as being unpatentable over Hung et al is requested in view of Amended Claims 1 and 15 and in accordance with the following remarks.

It is believed that the amendments to Claims 1 and 15 render the claims patentable over Hung et al. As discussed above, it is important that the dielectric constant of the entire dielectric layer be less than 2.5. This is achieved by using a low dielectric constant material without an etch stop layer. The dielectric constant of all portions of the dielectric layer is limited to less than 2.5 in amended claim 1 (see page 2). The absence of an etch stop layer is claimed in amended claim 15 (see bottom of page 10). There is no teaching or suggestion in Hung et al that an etch stop layer not be used, but such is a key feature of Applicants' invention.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 3, 5, 7, 8, 15-18, and 21-23 as being unpatentable over Hung et al is requested in view of Amended Claims 1 and 15 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 6, 19, 24-28, and 30 as being unpatentable over Hung et al in view of Tang et al is requested in view of Amended Claims 1, 15, and 24 and in accordance with the following remarks.

As discussed above, Hung et al does not teach or suggest not using an etch stop layer (as claimed in Claim 15) so that the dielectric constant remains lower than 2.5 (as now claimed in Claim 1). Claims 15 and 24 have been amended to claim that high polymer gases are not used in the first etching process (see pages 8-9 of the Specification). Claim 24 has been amended also to claim specific etching gases that are not to be used, as taught in the Specification. One of these gases, C_2F_6, is used by Tang et al (col. 9, line 52 – col. 10, line 3). Tang's etching recipe will cause spiking because of the presence of C_2F_6. Tang et al teaches away from Applicants' invention because Applicants have found that high polymer gases such as C_2F_6 cause spiking.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 6, 19, 24-28, and 30 as being unpatentable over Hung et al in view of Tang et al is requested in view of Amended Claims 1, 15, and 24 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 9 and 20 as being unpatentable over Hung et al in view of Chan et al is requested in view of Amended Claims 1 and 15 and in accordance with the following remarks.

It is agreed that Chan et al teaches a method similar to Applicants' method for etching the liner or lower stop layer. However, as discussed above, Hung et al does not teach or suggest not using an etch stop layer in the dielectric layer through which the damascene opening is to be etched (as claimed in Claim 15) so that the dielectric constant remains lower than 2.5 (as now claimed in Claim 1).

Reconsideration of the rejection under 35 U.S.C. 103 of Claims 9 and 20 as being unpatentable over Hung et al in view of Chan et al is requested in view of Amended Claims 1 and 15 and in accordance with the remarks above.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 29 as being unpatentable over Hung et al in view of Chan et al is requested in view of Amended Claim 24 and in accordance with the following remarks.

It is agreed that Chan et al teaches a method similar to Applicants' method for etching the liner or lower stop layer. However, as discussed above, Hung et al does not teach or suggest not using an etch stop layer within the dielectric layer through which the damascene opening is to be etched so that the dielectric constant remains lower than 2.5. Hung et al does not teach or suggest the particular etching gases used in the first etching, claimed in Claim 24.

Reconsideration of the rejection under 35 U.S.C. 103 of Claim 29 as being unpatentable over Hung et al in view of Chan et al is requested in view of Amended Claim 24 and in accordance with the remarks above.

Applicants have reviewed the prior art made of record and not relied upon and agree with the Examiner that while the references are of general interest, they do not pertain to the detailed claims of the present invention.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner K. Chen not find that the Claims are now Allowable that the Examiner call the undersigned at 765 4530866 to overcome any problems preventing allowance.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend the Claims as follows:

1. (TWICE AMENDED) A method of forming a damascene opening in the fabrication of an integrated circuit device comprising:

providing a contact region in or on a substrate;

depositing a liner layer overlying said contact region;

depositing a dielectric layer overlying said liner layer wherein [no] all portions of said dielectric layer [has] have a dielectric constant [higher] less than 2.5;

first etching said damascene opening through said dielectric layer to said liner layer overlying said contact region wherein said first etching comprises a high F/C ratio etch chemistry, high power, and low pressure; and

second etching said liner layer within said damascene opening to expose said contact region wherein said second etching comprises a high F/C ratio etch chemistry, low power, and low pressure to complete formation of said damascene opening in said fabrication of said integrated circuit device.

15. (TWICE AMENDED) A method of forming a damascene opening in the fabrication of an integrated circuit device comprising:

providing a contact region in or on a substrate;

depositing a liner layer overlying said contact region;

depositing a dielectric layer overlying said liner layer wherein said dielectric layer has a dielectric constant of less than 2.5 and wherein no etch stop layer is used within said dielectric layer;

first etching said damascene opening through said dielectric layer to said liner layer overlying said region to be contacted wherein said first etching comprises a high F/C ratio etch chemistry, power of 15 between 700 and 1000 watts, and pressure of between 20 and 150 mTorr and wherein a high polymer gas is not used; and

second etching said liner layer within said damascene opening to expose said region to be contacted wherein said second etching comprises a high F/C ratio etch chemistry, power of between 250 and 500 watts, and pressure of between 30 and 70 mTorr to complete formation of said damascene opening in said fabrication of said integrated circuit device.

24. (TWICE AMENDED) A method of copper metallization in the fabrication of an integrated circuit device comprising:

providing a contact region in or on a substrate;

depositing a liner layer overlying said contact region;

depositing a dielectric layer overlying said liner layer wherein said dielectric layer has a dielectric constant of less than 2.5;

first etching said damascene opening through said dielectric layer to said liner layer overlying said region to be contacted wherein said first etching comprises a high F/C ratio etch chemistry of CF_4, O_2, and Ar gases, power of between 700 and 1000 watts, and pressure of between 20 and 150 mTorr and wherein a high polymer gas comprising C_4F_8, CH_2F_2, C_2F_2, or C_2F_6 is not used;

second etching said liner layer within said damascene opening to expose said region to be contacted wherein said second etching comprises a high F/C ratio etch chemistry, power of between 250 and 500 watts, and pressure of between 30 and 70 mTorr;

depositing a barrier metal layer within said damascene opening;

depositing a copper layer overlying said barrier metal layer; and

polishing down said copper layer and said barrier metal layer to leave said barrier metal layer and said copper layer only within said damascene opening to complete said copper metallization in said fabrication of said integrated circuit device.